**Lab Experiment 2**

**Realization of Digital circuits using behavioral and Switch level**

**modeling**

**2.1 Objective:** To realize the design of digital circuits in Verilog using behavioral and switch level

modelling then simulating and synthesizing using EDA tools

**2.2 Software tools Requirement**

Equipments:

Computer with Xilinx and Modelsim Software Specifications: HP

Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk

Softwares: Synthesis tool: Xilinx ISE.

Simulation tool: ModelSim Simulator

**2.3 Prelab Questions**

*(write pre lab Q & A in an A4 sheet)*

1. Write the difference between initial and always block.

2. List the Reduction and Logical Operators.

3. Give the use of Blocking and Nonblocking statments.

4. Differentiate case, casex and casez statements.

**2.4.1 Problem 1:** Write a Verilog code to implement Flip flops.

The following points should be taken care of:

1. Use If statement to design positive edge triggered D flip

2. Use case statement to design negative edge triggered T flip flop

**2.4.2 Problem 2:** Write a Verilog code to implement Counters.

The following points should be taken care of:

1. Use behavioral model to design Up-Down Counter. When mode =’1’ do up counting and

for mode=’0’ do down counting.

2. Use behavioral model to design Mod-N counter.

3. Design SISO register using behavioral model.

**2.4.3: Problem 3:** Write a Verilog code to implement digital circuits using switch level

modelling.

1. Design inverter logic using verilog switch level modeling and verify the simulation result

using test bench.

2. Design two input CMOS NAND logic using verilog switch level modeling and verify the

simulation result using testbench.

3. Design 2:1 Mux using CMOS switches and write verilog coding using switch level

modeling and verify the simulation result.

**2.5 Post Lab :**

Write a Verilog HDL Code to implement a SIPO and PIPO shift registers.